AT76C901

WIRELESS VOIP PHONE

Implements on a single IC most functions of a wireless VoIP phone based on the IEEE 802.11b standard for wireless LANs.

Image: Postscriptum

- Supports 11 Mbit/s rates with automatic fallback to 5.5, 2 and 1 Mbit/s
- Enciphers/deciphers wireless data on-the-fly for maximum privacy
- Built around an ARM7TDMI™ processor for the H.323 protocol, TCP/IP, and phone functions
- Program cache for immediate code execution and reduced power consumption
- Integrated 6K x 32-bit and 2K x 32-bit internal SRAMs for fast code execution and temporary data storage
- Glueless external bus interface connects up to 64M bytes of SRAM, SDRAM or Flash memory
- Integrated 16-bit DSP connected to on-chip audio codec
- IEEE 802.11b standard wireless LAN interface
- Wireless LAN MAC unit built around second ARM7TDMI processor
- Glueless interface to external baseband processor
- USB, two USARTs, SPI and I^2C interfaces
- Two 400K sample/sec Analog-to-Digital Converters
- Six advanced counter/timers, watchdog timer
- 64-key (8 x 8 matrix) keyboard interface
- 4 x 4 LED matrix
- Minimum of 8 GPIO pins
- Low voltage 3.3V operation
- 208-pin PBGA package (23 mm x

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: (+1) (408) 441-0311
Fax: (+1) (408) 436 4200

Europe
Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
Tel: (+41) 26-426-5555
Fax: (+41) 26-426-5500

Asia
Atmel Asia Ltd
Room 1219
Chinachem Golden Plaza
77 Mody Road
Tsimshatsui East, Kowloon
Hong Kong
Tel : (+852) 272 19 778
Fax : (+852) 272 21 369

Japan
Atmel Japan KK
Tonetsu Shinkawa Bldg, 9F
1-24-8 Shinkawa
Chuo-Ku, Tokyo 104-0033
Japan
Tel : (+81) 3 3523 3551
Fax : (+81) 3 3523 7581

E-mail
literature@atmel.com

Web Site
http://www.atmel.com

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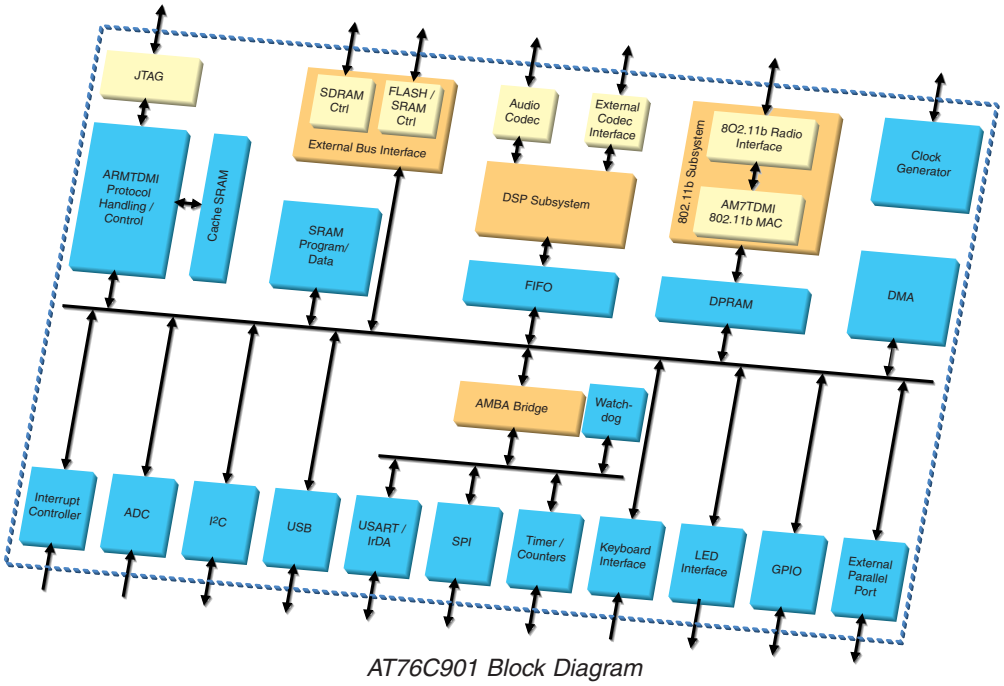
The AT76C901 integrates in a single IC the majority of functions of a battery-powered wireless phone that conforms to the IEEE 802.11b standard. Specifically, the first application of the device is targeted at an H.323 protocol-based wireless phone operating on an 802.11b wireless LAN at 2.4 GHz. It consists of the following subsystems:



AT76C901 Block Diagram

ARM7TDMI Main Processor

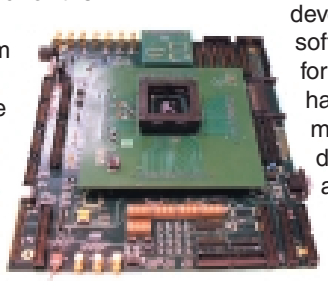
An embedded 32-bit ARM7TDMI™ RISC processor is used for overall system control, and to handle the H.323 and TCP/IP protocol stacks. It has a cache SRAM for immediate code execution, and accesses an on-chip SRAM for working code and data. Its external bus interface includes controllers for 8M bytes of external Flash, SRAM and SDRAM memories.

DSP Subsystem

The 16-bit DSP subsystem is connected to the system bus via transmit and receive FIFOs. It connects to an audio codec that provides the analog audio interface to the user. It is based on 16-bit linear ADC and DAC units.

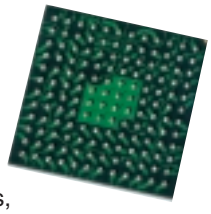
IEEE 802.11b Subsystem

The IEEE 802.11b subsystem contains a second ARM7TDMI processor that transfers data to or from the main system bus via a dual-port RAM (DPRAM). It also accesses the on-chip SRAM for working data. It executes the sophisticated firmware needed for the IEEE 802.11b MAC protocol. The IEEE 802.11b subsystem also incorporates a data encryption/decryption module that implements Wired Equivalent Privacy (WEP) RC4 for secure wireless connections.



The device implements the DES 64-bit encryption scheme in hardware, with the option of 128-bit DES encryption in software for added security.

Peripherals



The operational subsystems are supported by a wide range of on-chip peripherals. These include an interrupt controller, USB, two USARTs, SPI and I²C standard interfaces, six advanced counter/timers, and a watchdog timer to prevent system lockup. The GPIO and external parallel ports provide additional flexibility in the use of external I/Os. A DMA controller enables data transfers to and from certain peripherals without processor intervention.

Development Tools

An AT76C901 development board is available for evaluation and code develpopment. The embedded ARM7TDMI core is supported by a wide range of industry-standard application development tools. Application software modules are available for most standard protocol handling functions. This minimizes development time and reduces risk.